Implementations of Sintered Paste Vias In Printed Circuits Boards.

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High Performance Electronics Applications Require PCBs with High Aspect Ratio PTH

- Applications
  - High end computing
  - Semiconductor Test
  - Military

- PCB Design Trends
  - Increasing layer count
  - Increasing board thickness
  - Increased interconnect density
  - Signal integrity at high frequencies
Traditional Methods for Producing High Performance PCBs Result in Low Yield

- Outer-layer hole drilling yield
  - High aspect ratio drilling
  - Back drilling
  - Barrel plating
- Blind and buried vias
  - Multiple laminations
Blind and Buried Vias and Back-Drilling Technologies are Used to Increase Interconnect Density

Source: HDI Handbook, Happy Holden
Creating High-Aspect-Ratio PTH Boards from Interconnected Subassemblies Using Sintering Pastes is an Attractive Solution

- Interconnect core subassemblies using sintering conductive paste filled vias
- Thinner subassemblies
  - Small holes with high-yield aspect ratios
  - Higher current density can be used for PTH = higher throughput
  - Higher yield

Sintering pastes enable low cost, high performance PCB structures.

Source: Endicott Interconnect Technologies
Sintering Pastes Metallurgically Bond to Copper Catch Pads

Before Sintering

Copper and alloy particles in a liquid organic formulation

After Sintering

Sintered metal network

After lamination, sintered pastes will not remelt during solder reflow
Sintering Paste Can Be Used to Electrically Interconnect Multilayer Cores During Lamination
Filling Drilled Holes With Sintering Paste is Accomplished using Standard Printing Tools and Techniques

Industry standard stencil printing equipment is suitable for filling vias
Features of PCBs with Sintered Paste Core-to-Core Interconnects

- Break up high aspect ratio through holes
- Cores can be processed in parallel
- RoHS robust (reliable through lead-free reflow)
- Continuous metal joint – alloys to pads
- Substantially reduces plating time for high throughput
- High yields

Source: DDI
Cores are interconnected by sintering paste in the conventional prepreg lamination process.
### 3rd Party Interconnect Reliability Data Shows Sintering Pastes Meet Requirements

<table>
<thead>
<tr>
<th>Test</th>
<th>Test Conditions</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal shock</td>
<td>-55°C – 125°C, 500 cycles</td>
<td>Pass, Max resistance change 7.5%</td>
</tr>
<tr>
<td>Temp Cycling</td>
<td>0-100°C, 1000 cycles</td>
<td>Pass</td>
</tr>
<tr>
<td>Humidity + bias testing</td>
<td>85°C, 85RH%, 50V bias, hold 240 hrs</td>
<td>Pass</td>
</tr>
<tr>
<td>Humidity + Thermal Aging</td>
<td>85°C, 85RH%, hold 1000hrs</td>
<td>Pass, Max resistance change 4.0%</td>
</tr>
<tr>
<td>High Temperature Storage</td>
<td>150°C, hold 1000h</td>
<td>Pass, Max resistance change 7.0%</td>
</tr>
<tr>
<td>Solder reflow test</td>
<td>Reflow @ 260°C, 5 cycles</td>
<td>No delamination</td>
</tr>
<tr>
<td>Electrical test</td>
<td>No shorts or opens</td>
<td>Pass</td>
</tr>
</tbody>
</table>

Sintering paste interconnects are well established in HDI and high layer PCB applications.
Sintering Pastes Have Robust Electrical Results in High Layer Count Applications

Insertion loss of nets with and without sintered interconnects demonstrate a negligible difference over a wide frequency range.

Sintered Paste Interconnects can Lower Costs of High Layer Count PCBs

• Cost Savings
  – Elimination of outer-layer drilling
  – Higher yield from reduced aspect ratio plating
  – Higher yield from known good cores
Sintered Paste Vias Support a Wide Range of Interconnect Pitch

- Sintered paste microvias
- Core dimensions:
  - Ø125-250 µm
  - 75 µm
- Pitch range:
  - 0.4-2 mm
  - 200-400 µm
  - 40-45 µm
Laser Drilling of Prepregs is a Critical Process to Ensure Robust Paste Interconnection

Laser ablation of prepreg requires very different parameters than forming vias in cured laminate
Sintered Paste Microvias are a Cost-Effective and Reliable Alternative to Plated Microvias

- Circuit layers are fabricated in parallel
- Microvia interconnections can all be formed in a single lamination cycle
- No plated microvias are required
- Mixed configurations – PTH, plated microvia, sintered paste microvia – are supported
Prepreg Selection is Critical to Prevent Voids After Lamination

Sintering paste vias are compatible with standard adhesion promoter coatings and lamination cycles.
How to Implement Sintered Paste Microvias:
10-Layer, 0.4 mm Pitch, all Sintered Paste
Microvia Example

Etched foil    Sintered paste microvias

675 µm (27 mil)  400 µm  280 µm

125 µm  125 µm  9 µm  65 µm
Cores With Sintered Paste Microvia Layers are Aligned and Laminated

Each 2-layer core is exposed to two laminations. Shrinkage is consistent throughout the part.
How to Implement Sintered Paste Microvias: 10-Layer, 0.4 mm Pitch, Mixed Microvia Example

Etched circuits/pads

Sintered paste microvias

Plated closed microvias

~900 µm (36 mil)

400 µm

250 µm

100 µm

12 µm foil + ~15 µm panel plating

75 µm

100 µm
Summary: Core-to-Core Implementation of Sintered Paste Vias

- Electronic devices addressing high end computing, ATE, and military applications can require high layer count PCBs with blind and buried vias
- Increasing interconnect density requirements are pushing designs to utilize low yielding high-aspect-ratio PTHs
- High aspect ratio PTHs require complex drilling and plating processes, and frequently add cost to the PCB through low yield
- Breaking high-aspect-ratio through holes up by manufacturing and interconnecting subassembly ‘cores’ using paste interconnects is an alternative technology to plating high aspect ratio PTHs
- Sintering conductive pastes are a reliable interconnect solution for complex PCBs and enable lower costs, and higher yield compared to plating
- Customer products and third party test vehicles suggest sintered paste interconnects are viable for the manufacture in multiple lamination, high aspect ratio, printed circuit boards
Sintered Paste Microvias for HDI PCBs

- Cost savings
  - Capital equipment: reduce requirement for additional plating lines
  - Cycle time
  - Yield
- Proven reliability
- Versatility